IS RL101 Winchester Disk Controller
Hardware Reference Manual

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FCC WARNING

Class A Computing Devices

This equipment generates, uses, and may emit radio frequency energy. The equipment has been type tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such radio frequency interference when operated in a commercial environment. Operation of this equipment in a residential area may cause interference in which case the user at his own expense may be required to take measures to correct the interference.

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PREFACE

This manual describes the features, specifications, configurations and use of Integrated Solutions' RL101 Winchester Disk Controller. Installation and elementary troubleshooting information is provided. The programming of the registers of the RL101 is included, highlighting where the programming differs from the DEC* RLV11 and RLV12 controllers.

The manual is divided into six sections.

SECTION 1 is the introduction and presents the general features of the IS RL101.

SECTION 2 lists the specifications.

SECTION 3 describes RL Mode Operations.

SECTION 4 describes Extended Mode Operations.

SECTION 5 contains installation instructions and describes disk subsystem operations.

APPENDIX A lists disk parameters for selected drives.

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SECTION 1: GENERAL DESCRIPTION

1.1 Introduction

The RL101 Winchester Disk Controller is a 5 1/4" disk controller/formatter that meets the LSI-11 bus specifications (DECSTD 160.) The single quad-sized card plugs into any LSI-11 bus-compatible microcomputer, forming the heart of a disk subsystem with up to four 5 1/4" Winchester disk drives.

The RL101 operates in two modes. In *RL Mode*, the controller emulates DEC RLV11 (18-bit LSI-11 Bus) or RLV12 (22-bit LSI-11 Bus) disk controllers, controlling up to four RL01- or RL02-emulating disk drives. In this mode, the maximum storage capacity of an RL101 disk subsystem is 41.6 megabytes.

In *Extended Mode*, the controller does not emulate any standard directly, although it is equally compatible with 18-bit and 22-bit LSI-11 bus systems. In this mode, the RL101 controls up to four disk drives, each with a capacity of up to 524 megabytes. Thus, the maximum disk subsystem capacity increases to 2.1 gigabytes in Extended Mode.

The controller is designed to communicate with multiple drives in a time-shared fashion. Connections between the controller and drives are made in radial/serial mode. That is, a single 20-pin ribbon cable containing the high-speed serial data connects the controller with each disk drive and a 34-pin ribbon cable containing the control information connects the controller to the drives in daisy-chain fashion.

1.1.1 Control Microprocessor

The RL101 uses a high-speed 16-bit microprocessor to control almost all operations. This microprocessor handles the LSI-11 bus interface in addition to the control signals to the attached 5 1/4" Winchester drives. It also participates in the data transfer between the on-board buffer and the Winchester drives.

Use of a 16-bit microprocessor makes the controller intelligent: it handles completely functions that commonly require host participation with less intelligent controllers, including disk formatting, disk bad spot mapping, retries, and error detection and correction.

1.1.2 Buffer RAM

All information is transferred between the disk and the LSI-11 bus memory through the on-board buffer, preventing data late problems. Such problems can occur with non-buffered controllers when a FIFO overflows and the controller cannot get the LSI-11 bus disk fast enough to prevent data loss. The on-board buffer is up to 15 sectors long which means that a whole RL01/2 track of 40 sectors is transferred in two and a half 5 1/4" disk revolutions.

1.1.3 EPROMS

A set of two 2716-1 type EPROMs (Table 1-1) determine the controller mode of operation and the specific disk subsystem configuration. The controller EPROMs, located at board locations 6J and 10J, are clearly marked.

Table 1–1. RL101 EPROMS

PROMs	Function
	RL Mode
RL101	Allows up to four R01s *or* four RL02s to be emulated on four physical drives
2L	Allows four RL02s to be emulated on two physical drives, *or* two RL02s to be emulated on one physical drive. DL0 and DL1 always appear on drive 0; DL2 and DL3 always appear on drive 1.
4L	Allows up to four RL02s to be emulated on one drive, drive 0.
	Extended Mode
EXM.x	Provides extended mode support for up to four drives. Each drive can have up to 16 heads and 2048 cylinders. The EXM3.x EPROMS replace the EXM2.x EPROMS, which provide extended mode support for up to four drives, each with up to eight heads and 1024 cylinders.

1.1.4 LSI–11 Bus Interface

The bus interface logic handles all DMA and interrupt protocol and data transfers between the controller and the LSI-11 bus. The bus interface employs DEC-approved bus drivers, receivers and transceivers and is compatible with either the 18-bit or 22-bit LSI-11 bus.

1.1.5 Serialiser/Deserialiser

The serializer/deserializer (SERDES) hardware converts 16-bit parallel information into the high-speed serial data stream required by the disks and converts the high-speed serial stream from the disks into 16-bit- parallel information.

1.1.6 Error Detection and Correction

An AMD burst error processor (BEP) is employed to generate four-byte syndromes that are appended to the ends of the header and data fields on each sector on the disk during formatting and disk write operations. During read operations, the BEP reads the header and data information in parallel with the SERDES unit and recalculates the syndrome. If the calculated syndrome does not agree with the syndrome from the disk, the control microprocessor is notified that the information loaded into the on-board buffer is not correct. The control microprocessor retries the operation eight times. If one of the retries is successful, the controller resumes execution of the command. If the retries are unsuccessful, the control microprocessor manipulates the BEP in such a manner to get a correction word to correct the information in the on-board buffer if it is correctable by the BEP. If the BEP cannot correct the data, the operation is terminated and the host is made aware of the existence of a hard data CRC.

1.1.7 Phase-Locked Loop

Information on 5 1/4" Winchester disks is recorded in MFM format. The function of the phase-locked loop is to separate the data and clock streams which are combined in the MFM format. A crystal-controlled phase-locked loop is used to recover data and clock information from the MFM format.

1.1.8 Addressable Registers

The controller contains five word-addressable registers:

Control Status Register (CSR)
Disk Address Register (DAR)
Bus Address Register (BAR)
Word Count/Multipurpose Register (WCR)
Bus Address Extension Register (BAE)

Each register has a read/write capability. A complete description of the register configurations and functions can be found in Section 3 (for RL Mode) or in Section 4 (for Extended Mode.)

1.1.9 Commands

The controller supports several commands:

Write Check
Get Status
Seek
Get Seek Status (Extended Mode only)
Read Header
Write (with Implied Seek in Extended Mode)
Read (with Implied Seek in Extended Mode)
Read Data Without Header Check (RL Mode only)
Format
Read Bad Track Map

1.2 Subsystem Configurations

An RL101 disk subsystem can have up to four drives per RL or Extended Mode controller. Two controllers per system are supported. RL Mode and Extended Mode controllers can be co-resident, provided they do not occupy the same register addresses. As shipped from the factory, the controllers have the same device addresses. Therefore, the address of one of them will have to be adjusted, if two controllers will be configured in one system. Refer to Section 3.

1.2.1 RL Mode

In RL mode (18- or 22-bit LSI-11 bus system), each drive can store 5.24 megabytes of information when emulating an RL01 disk, and 10.48 megabytes when emulating an RL02 disk. Either type drive can be mixed on the same controller as can drives with different numbers of heads.

In this mode, the maximum storage capacity of an RL101 disk subsystem is 41.6 megabytes in one of these configurations:

four drives emulating four RL02s

two drives, each emulating two RL02s

one drive emulating four RL02s

This storage capacity limitation in RL mode is imposed by the DEC RLV11 and RLV12 controllers, which the RL101 emulates. These controllers support up to four RL01/02 drives only.

1.2.2 Extended Mode

In Extended Mode (18-bit or 22-bit LSI-11 bus system), the RL101 controls up to four disk drives, each with a capacity of up to 524 megabytes. Thus, the maximum disk subsystem capacity increases to 2.1 gigabytes in this mode.

SECTION 2: SPECIFICATIONS

2.1 Processor and Bus

The RL101 bus is LSI-11 bus compatible and meets all requirements of DEC STD 160 with 18 or 22 bit addressing.

2.2 Device Addresses

The RL101 interface is the same as that provided by the DEC RLV11 and RLV12 controllers and consists of five registers at the indicated addresses*:

17774400 - Control Status Register
17774402 - Disk Address Register
17774404 - Bus Address Register
17774406 - Word Count/Multipurpose Register
17774410 - Bus Address extension Register

The commands recognized by the subsystem are identical to those of the DEC RLV11/12.

2.3 Interrupt Vector

160(8) standard, settable by user

2.4 Transfer Rate

1.2 Mbytes/sec burst

2.5 Power Requirements

+5v - 2.5 amps
+12v - .05 amps
(both from LSI-11 backplane)

2.6 Environmental

Temperature: 0 ° C to 50 ° C (operating)
-40 ° C to 65 ° C (non-operating)

Humidity: 10% to 90% (non-condensing)

2.7 EPROMS

Two 2716-1 type EPROMs.

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* These are the default addreses for these registers; they are different when the RL101 jumpers J1-J6 are reconfigured. See Section 3.

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SECTION 3: RL MODE

3.1 Introduction

Section 3 addresses the configuration and programming of the RL101 controller in RL mode.

3.2 Jumper Configurations

The RL101 Winchester Disk Controller has been configured at the factory to meet the most common set of user needs. In some cases, however, the RL101 jumper configurations must be reconfigured before operation, as described in the following paragraphs.

NOTE

No reconfiguration is required to use disks with different numbers of heads and cylinders. This information is specified at format time, permanently retained on the disk after format and read into the controller at power-up time.

3.2.1 Addressing Jumpers J1–J6

The addressing jumpers (J1-J6) select the address range to which the RL101 responds. There are four possible configurations: two of the configurations cause the RL101 to look like the first or second RLV11 controller in an 18-bit LSI-11 system; the two remaining configurations cause the RL101 to look like the first or second RLV12 in a 22-bit LSI-11 system. The factory setting causes the controller to emulate the first RLV12 in a 22-bit LSI-11 system. This factory setting also applies to Extended Mode operations.

Table 3-1 summarizes the available configurations along with the applicable register addresses, which are described in the following paragraphs.

The addressing jumpers are numbered from J1 to J6 as shown in Figure 3-1.

3.2.2 22–Bit Addressing Jumper Configurations

The RL101 can be configured to look like either the first or second RLV12 controller in a 22-bit LSI-11 bus system. In 22-bit mode, 5 registers are accessible in the RL101: the CSR, BAR, DAR, WCR and the BAE, the Bus Address Extension register which holds the top six bits of the 22-bit LSI-11 address. As the first controller, the RL101 responds to addresses, 17774400-17774410(8). As with the RLV12, the RL101 also responds to addresses 17774412-17774416(8) as dummy addresses. Reading any of these addresses gives the current contents of the BAE register.

To configure the RL101 to look like the first RLV12 in a 22-bit LSI-11 system, connect:

J1-J2, J4-J5 (factory setting)

J3 and J6 remain unconnected.

To configure the RL101 as the second controller in a 22-bit LSI- 11 system (adresses 17774420-17774430(8)), connect:

J1-J6, J2-J4-J5.

J3 remains unconnected.

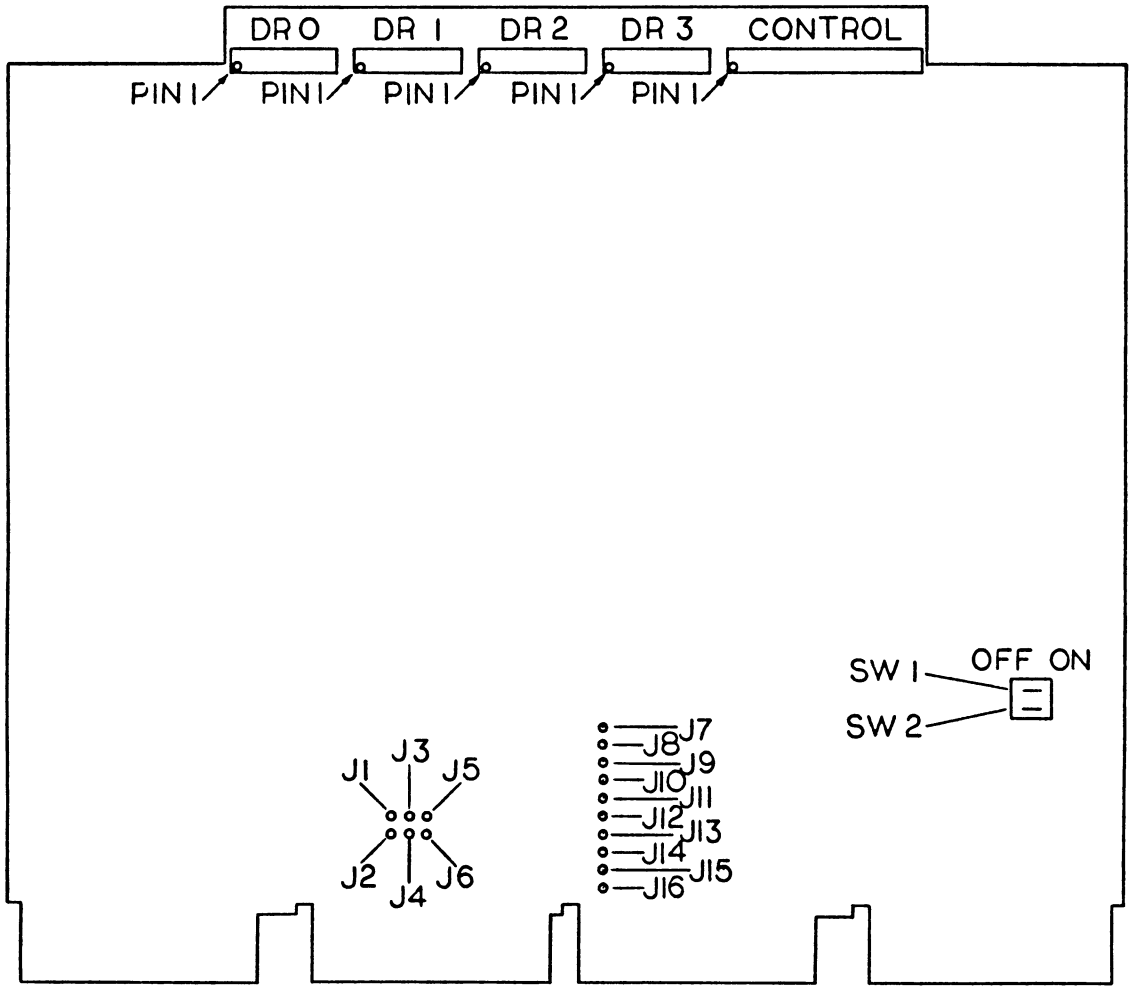

Figure 3–1. Jumper/Switch Locations

3.2.3 18-Bit Addressing Jumpers Configurations

In 18-bit mode, the RL101 responds to only four registers addresses: the CSR, BAR, DAR and WCR. When the RL101 is the first RLV11 in an 18-bit LSI-11 system, these registers are at addresses 774400-774406(8).

To make the RL101 look like the first RLV11 in an 18-bit LSI-11 system, connect:

J1-J2, J3-J4.

J5 and J6 remain unconnected.

As the second RLV11, the RL101 responds to addresses 774420-774426(8). To configure the RL101 for operation in this manner, connect:

J1-J6, J3-J4, J2-J5.

Table 3-1. Addressing Jumper Configurations/Register Addresses

Configuration	Setting	Register Addresses
RLV12/22-Bit LSI-11 Bus		
First RL101*	J1-J2 J4-J5 (J3,J6 remain unconnected)	17774400-17774410(8) 17774412-17774416(8) (dummy)
Second RL101	J1-J6 J2-J4-J5 (J3 remains unconnected)	17774420-17774430(8) 17774432-17774436(8) (dummy)
RLV11/18-Bit LSI-11 Bus		
First RL101	J1-J2 J3-J4 (J5,J6 remain unconnected)	774400-774406(8)
Second RL101	J1-J6 J3-J4 J2-J5	774420-774426(8)

* This is the factory configuration for both RL and Extended Mode controllers.

3.2.4 Interrupt Vector Jumpers

As shipped from the factory, the RL101 is configured for vector 160(8). The vector can be changed by changing the wiring on wire wrap posts J7-J16 in the following manner. Wirewrap post J7 corresponds to a logic low and wirewrap post J16 corresponds to a logic high. The remaining jumpers correspond to the following vector addresses:

J8 - DAL 4
J9 - DAL 6
J10 -DAL 7
J11 -DAL 2
J12 -DAL 8
J13 -DAL 1
J14 -DAL 3
J15 -DAL 5

To configure for a particular vector address, those jumpers that are logic 1 in the vector address should be tied to J16 and those jumpers that are logic 0 should be tied to J7.

For example, vector 160(8) is set by tieing J8, J9, J15 to J16 and the remaining jumpers to J7.

3.3 User-Modifiable Parameters

For added flexibility, the sophisticated user can change three additional parameters by modifying the contents of three locations in the low-order EPROM located at board location 10J.

NOTE

The RL101 disk controller requires 2716 type EPROMS with an access time of 350 ns or better. These are usually referred to as 2716-1 and 2716H EPROMS by various manufacturers. It is strongly recommended that the user retain his original EPROM as a backup when making changes.

3.3.1 Transfer Block Size

The Transfer Block Size (memory location 5(8)), the number of words the RL101 transfers each time it becomes bus master, is programmable from two to 256 words. For RL Mode, the default value in the EPROMs as configured by the factory is 16 words per burst. Performance of the RL101 can be improved by as much as 20% in some applications by using a longer DMA burst. To use very long bursts, above 64 words per burst, be sure that no other devices in the system will lose data while the RL101 is bus master. The RL101 will occupy the bus as bus master for a period of time according to the following formula:

6 microseconds + (1.8 microseconds/word * words per burst).

This excludes DMA latency and memory access times above 200 ns. For memories with access times between 200 and 400 ns., the 1.8 multiplier is replaced with 2.0 microseconds/word.

3.3.2 Step Time

The RL101 controller is designed for use with buffered step mode 5 1/4 " Winchester disks. All of the Winchester disks in production today with the exception of the ST506 and the Texas Instruments version of the ST506 employ a buffered step interface. The RL101 can issue steps at rates from 10 - 64,000 microseconds per step.

The step rate can be changed by changing location 4(8) of the low-order EPROM according to the following formula:

10 + N microseconds per step

where N is the quantity placed in location 4(8).

The factory-configured step rate is 10 microseconds/step (0 in location 4(8)), which is compatible with almost all of the 5 1/4" Winchester drives currently in production.

3.3.3 Maximum Number of Spared Tracks

The RL101 and 2L EPROM versions of the firmware allow a maximum of 12 spared tracks per disk while the 4L EPROM version allows a maximum of 34 spared tracks per disk. For the RL101 and 2L PROMs, location 6(8) is factory set to 12; for the 4L EPROMs, location 6(8) is factory set to 34. This location can be set to less than 12 or 34 in special cases, such as when there are less than 12 or 34 spared tracks available, but in no case should it be set higher than the firmware handling capacity.

3.3.4 Firmware Revision Level

The Firmware Revision Level (memory location 3(8)) contains two hex digits which represent the firmware revision level. This information should not be changed by the user.

3.4 Addressable Registers

The RL101 disk controller has five addressable registers (Table 3-2.) They are used to store data and control information. These registers can be accessed like any location in memory except that they may not be read or written while the controller is busy. In an LSI-11 system, the upper 8K bytes of address space is reserved for I/O device addresses. Each RL101 register has a unique address assigned within this range.

Table 3-2. Register Addresses*

LSI-11 BUS	
Octal Address	Register Name
17774400	Control Status Register
17774402	Bus Address Register
17774404	Disk Address Register
17774406	Word Count Register
17774410	Bus Address Extension Register

NOTE

Only the lower 12 bits of the addresses are decoded. The upper 10 bits are asserted with the signal BANK SEL 7.

3.4.1 Control Status Register

The control status register (CSR) is a 16-bit word- address of 17774400. Bits 1 through 9 can be read or written. The remaining bits can only be read. See Tables 3-3 and 3-4 for the description of the bit format of the Control Status Register.

* These are the factory-set register addresses. They are different if Address Jumpers J1-J6 are reconfigured. Refer to Table 3-1.

Table 3-3. CSR Bit Description (Bits 0-9)

Bit(s)	Function	Description
0	Drive Ready (DRDY)	When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a disk operation is initiated. It is set when the operation is completed.
1-3	Command Code	These bits are set by software to indicate the command to be executed.
	Command:	F2-F0
	No Op (RL11) or Maintenance mode (RLV11/RLV12)*	000
	Write Check	001
	Get Status	010
	Seek	011
	Read Header	100
	Write Data	101
	Read Data	110
	Read Data Without Header Check	111
4-5	Bus Address Extension Bits (BA16, BA17)	The two most significant bus address bits, when operating in 18-bit addressing mode. Read and written as data bits 4 and 5 of the CSR but considered as address bits 16 and 17 of the BAR.
6	Interrupt Enable (IE)	When this bit is set by software, the controller is allowed to interrupt the processor at the normal command or error termination of a command.
7	Controller Ready (CRDY)	When cleared by the software, this bit indicates that the command code in bits 1-3 is to be executed (negative GO bit). When set, this bit indicates that the controller is ready to accept another command.
8-9	Drive Select (DS0, DS1)	These bits determine which drive will communicate with the controller.

* Used for the Format and Read Bad Track Map Commands on the RL101 controller.

Table 3-4. CSR Bit Description (Bits 10-15)

Bit(s)	Function	Decription
10-13	Error Code	Error Code/Name - E13-E10 0001 - Operation Incomplete 0010 - Read Data CRC or Write Check Error 0011 - Header CRC (HCRC) Error 0100 - Date Late (DLT) (Impossible on RL101) 1000 - Non-Existent Memeory 1001 - Memory Parity Error (not supported on RL101)
14	Drive Error (DE)	The source of the error can be determined by executing a Get Status command and then executing an WCR read. DE can be cleared by executing a Get Status command with bit 3 of the DAR.
15	Composite Error	When set, this bit indicates that one or more of the error bits (bits 10-14) is set. If the IE bit (bit 6 of CSR) is set, and an error occurs, an interrupt will also be initiated.

3.4.2 Bus Address Register

The Bus Address Register (BAR) is a 16-bit word-addressable register with an address of 17774402. Bits 1 through 15 can be read or written. Bit 0 is always zero. Bus address bits 16 and 17 are contained in bits 4 and 5 of the CSR.

The BAR indicates the memory location involved in the data transfer during a normal read or write operation. The contents of this register are automatically incremented by two as each word is transferred between the bus and the I/O buffer. This BAR overflows into CSR bits 4 and 5; it is cleared by initializing the controller and loading the register with zeroes. The bit format of the BAR is described in Table 3-5.

Table 3-5. BAR Bit Description

Bit(s)	Description
0-15	These bits point to the memory address to/from which data is to be transferred. Bits 16 and 17 are in CSR bits 4 and 5. If the RL101 is in 22-bit mode, bits 16 through 21 can be found in the BAE regester.

3.4.3 Disk Address Register

The Disk Address Register (DAR) is a 16-bit register with an address of 17774404. Its contents can have one of three meanings depending on the command (Seek, Read or Write, Get Status) being performed. This register is cleared by initializing the device or loading the register with zeroes. All 16 bits can be read or written by the processor.

3.4.4 Word Count Register

In RL Mode, the Word Count Register (WCR) is a write-only register that holds the word count in two's complement form for read and write operations. Bits 0-12 hold the total number of words to be transferred (in two's complement); bits 13-15 must be one.

3.4.5 Bus Address Extension Register

The Bus Address Extension Register (BAE) has one function in RL Mode. The bottom six bits of this register provide the upper six bits of the 22 bit LSI-11 bus address.

3.5 Command Descriptions

RL Mode supports these commands

Write Check
Get Status
Seek
Read Header
Write
Read
Read Data Without Header Check
Format
Read Bad Track Map

which are described in the following paragraphs.

3.5.1 Write Check Command

The Write Check command reads data off the disk and compares it with the data in memory in the same manner that the RL02 Write Check command operates. Before issuing Write Check, the following information must be provided:

- Memory Address at which the comparison is to take place. This is specified in the BAR and the bottom six bits of the BAE or bits 4 and 5 of the CSR, depending upon whether the controller is in 18-bit or 22-bit mode.
- Disk Address at which the comparison is to take place. This is specified in the DAR.
- Length of the transfer in words. This is specified as a two's complement number in the WCR.

3.5.2 Get Status Command

For a Get Status command, the DAR bits must be programmed as shown in Table 3-6.

Table 3-6. DAR During Get Status Command

Bit(s)	Function	Description
0	Marker Bit	Must be 1.
1	Get Status(GS)	Must be a 1, indicating to the drive that the status word is being requested At command completion, the drive status word is read into the WCR. With this bit set, bits 8-15 are ignored.
2		Must be 0.
3	Reset(RST)	When this bit is set the drive clears its error register (resets all drive faults) before sending the status word to the controller.
4-7		Must be 0.
8-15		Not used.

3.5.3 Seek Command

The Seek Command allows seeks to take place without read or write operations. The command is issued with the destination logical track number put into the DAR. Note that the Seek Command returns immediately after the seek has been initiated, but before it completes. Table 3-7 shows the contents of the DAR during a Seek command.

Table 3-7. DAR During Seek Command

Bit(s)	Function	Description
0	Marker Bit	Must be a 1.
1	Seek	Must be a 0, indicating to the drive that a seek is being requested. With this bit cleared, the drive uses the remaining contents of the register as seek parameters.
2	Direction (DIR)	This bit indicates the direction in which a seek takes place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-15).
3		Must be a 0.
4	Head Select (HS)	Indicates which head (disk surface) is to be selected. A one selects the lower head. A zero selects the upper head.
5-6		Reserved
7-15	Cylinder Address Difference DF 08:00	Indicates the number of cylinders the heads are to move on a seek.

3.5.4 Read Header Command

The Read Header Command reads the first header that comes under the currently selected head of the selected drive and places the second header word in the BAR and the third header word in the DAR. The second header word contains the Cylinder Number in bits 15-6 and the Sector Number in bits 5-0. The third header word contains the Head Number in bits 15-13 and the Logical Track Number in bits 12-0.

3.5.5 Write Command

The Write command writes information from memory onto the disk. The user must specify the starting Memory Address, the Disk Address and the Word Count in the same manner as with the Write Check command.

3.5.6 Read Command

The Read Command reads information from disk into memory. The user must specify the starting Memory Address, the Disk Address and the Word Count in the same manner as with the Write Check command.

3.5.6.1 DAR During Read or Write Data Command

For a read or write operation, the DAR is loaded with the address of the first sector to be transferred. As each successive sector is transfered, the DA register is automatically incremented. The contents of this register are used by the header comparison logic to locate the desired sector. The header read from the disk is compared against the contents of this register. Table 3-8 describes the bit format.

Table 3-8. DAR During Data Transfer Commands

Bit(s)	Function	Description
1-5	Starting Sector Number (SA)	
6	Head Address(HA)	Desired head address of one of the two drive heads. A one indicates the lower head; a zero, the upper head.
7-15	Cylinder Address (CA) 08:00	Desired address of one of the cylinders on the disk (range is 0 through 777, octal).

3.5.7 Read Data Without Header Check Command

This command reads the first header encountered on the selected drive. The header gives cylinder, sector, and selected head information. This information is used by the software in calculating an address for the Seek command.

3.5.8 Format Command

The Format and Read Bad Track Map Commands replace the RLV12 Maintenance command. The Format Command formats a drive in a single operation. The format parameters for the drive to be formatted are written to the DAR; then the Format Command (Command 0) is written to the CSR and the GO bit is reset. Tables 3-9 and 3-10 show the contents of the DAR when formatting with the RL101/2L EPROMs and the 4L EPROMs. Refer to Section 5 for more information on the operational aspects of formatting drives attached to the RL101 controller.

Table 3-9. DAR During Format Command (RL101/2L EPROMs)

Bit	Contents
Bits 0-2	the number of heads on the drive being formatted minus one. A maximum of 8 heads can be supported by the RL101. For example, for a drive with four heads, the number that is entered in bits 2-0 is three.
Bits 3-12	the number of the maximum cylinder on the drive being formatted. The RL101 supports drives with a maximum of 1024 cylinders.
Bit 13	not used
Bit 14	1- RL02 emulation will be performed on the disk being formatted. 0-RL01 emulation will be performed on the disk being formatted.
Bit 15	1-Format command

NOTE

When formatting completes, information about whether an RL01 or RL02 is being emulated and the number of heads is preserved on the disk along with the track sparing information. The maximum number of cylinders is used during formatting only.

Table 3-10. DAR During Format Command (4L EPROMs)

Bit(s)	Definition
Bits 9-0	The number of the maximum cylinder on the drive. When specifying this parameter, it is not necessary to allocate tracks at the end of the drive as spared tracks; the controller automatically does this. This number should be the actual largest physical cylinder number on the drive. 1023 decimal is the largest number that can be specified.
Bits 12-10	The number of the maximum head on the drive, minus one. Drives with up to eight heads are supported. For a drive with eight heads, the number would be 7.
Bit 13	Putting a one into this bit allows the user to examine the progress of formatting by examining a memory buffer beginning at location 10000(8) in physical memory. If bit 13 is set, the controller allocates a 69 word buffer starting at 10000(8) for status information. The layout of the buffer is defined in Table 5-1.
Bits 15-14	not used, must be zero during formatting.

3.5.9 Read Bad Track Map Command

The Read Bad Track command allows the user to view the hardware bad track map generated by the controller at format time and stored on the disk.

The Read Bad Track Command shares command 0 in the controller CSR with the Format command. The two commands are differentiated from each other in the controller by means of bit 15 of the DAR. For the RL and 2L PROMs, the Read Bad Track command is executed by writing a 0(8) in location 17774404 (DAR) and then writing a 0(8) in location 17774400 (the CSR.) For the 4L EPROMs, write all ones to location 17774404. Table 3-11 shows the DAR during a Read Bad Track Map Command.

The Read Bad Track Map command dumps the bad track map of any drive attached to the controller to a 69-word memory buffer beginning a location 10000(8) for examination by the host computer. Table 3-12 shows the format of the Bad Track Map for the RL101 and 2L EPROMs; Table 3-13 shows the format for the 4L EPROMs. Frequently, no bad tracks are found on a Winchester disk during formatting. In this case, all entries in words 2-13 (words 2-69 for the 4L EPROMs) of the bad track map will be filled with 177777(8).

NOTE

DEC bad sector sparing area. The last track on the RL01 and RL02 disk is reserved for bad sector sparing information by Digital. The RL101 writes this area during formatting in such a way to indicate that no bad sectors exist on the disk. This area can be updated by operating system software in a completely compatible way with the RLV11/RLV12.

Table 3–11. DAR During Read Bad Track Map Command

Bit(s)	Description
14-0	Don't care.
15	0 - RL and 2L EPROMs. 1 - 4L EPROMs.

Table 3–12. Bad Track Map (RL/2L PROMs)

Location	Function	Contents
10000(8)	Disk Parameter Word (Word 1)	Bit 15: 0 - RL01 emulation Bit 15: 1 - RL02 emulation Bits 14-3: 0s Bits 2-0: Number of heads minus one.
10002(8) 10004(8) ... 177777(8)	Bad Track Map Words (Words 2-13)	Bits 15-12: offset to be added to a logical track to get a physical track Bits 11-0: the logical track above which the offset in Bits 15-12 is to be added. End of the bad track map.

Table 3-13. Bad Track Map (4L EPROMs)

Location	Function	Contents
10000(8)	Disk Parameter Word (Word 1)	Bits 15-13: number of heads minus one Bits 12-0: number of logical tracks available (number of cylinders x number of heads - maximum number of tracks which could be spared.)
10002(8) 10004(8) ...	Bad Track Map Words (Words 2-69)	Each bad track occupies two word locations. The first location is the logical track which is spared. The second is the offset.
177777(8)		End of bad track map.

SECTION 4: EXTENDED MODE OPERATIONS

4.1 Introduction

This section describes Extended Mode operation on the RL101 disk controller. Extended Mode operation supports:

- 5 1/4 inch Winchester drives with large capacity
- Multiple drives with varying capacities on the same controller
- Implied seeks
- Automatic crossing of track/cylinder boundaries.

Large Capacity Disks

In Extended Mode, drives with up to 2048 cylinders and up to 16 heads are supported. This gives a maximum drive size of 32768 tracks per drive with each track containing up to 32 512 byte blocks. Thus, the controller supports up to four drives, each with up to 524 megabytes formatted capacity. Note that the sector size of the Extended Mode RL has been increased to 512 bytes to make it compatible with most of the other Digital Equipment Corporation disk drives.

NOTE

Extended Mode EXM2.x PROMs support only drives with up to 1024 cylinders and up to eight heads.

Multiple Drives

The Extended Mode firmware uses a mechanism whereby the number of heads, cylinders and tracks on the drive are stored on the drive at the completion of the formatting operation and are automatically read into the controller at power-up. The system software simply accesses the drives as a number of logical tracks; conversion of the track number to a cylinder and head number is performed by the controller taking into account the bad track sparing map. The host can determine the number of logical tracks available on each drive attached to the controller by issuing the Get Status command.

Implied Seeks

In RL mode, the controller must perform a separate seek operation to get the drive to the correct cylinder before a read or write operation can be performed. This results in extra overhead and twice as many interrupts for a given operation. With the Extended Mode EPROMs, a read or write operation can be given to any logical track and if a seek is necessary to get to the correct cylinder, the controller automatically performs it in a transparent fashion, taking into account the bad track sparing map.

Automatic crossing of track and cylinder boundaries

The Extended Mode RL101 will automatically cross track and cylinder boundaries with a single command. The WCR (word count register) functions exactly the same as for the standard RL02, except that the longest transfer is now 64K words, indicated by a word count of zero.

4.2 Jumper Configurations

4.2.1 Addressing Jumpers J1–J6

The RL101 controller is shipped from the factory jumper configured to emulate an RLV12 in 22-bit LSI-11 mode. It is equally compatible with 18-bit LSI-11 busses. For Extended Mode operation, this factory setting need not be changed unless the controller is to appear as the *second* RL101 on the bus in which case the jumpers will have to reconfigured on the second controller. Refer to Table 3-1.

4.2.2 Interrupt Vector Jumpers

When shipped from the factory, the RL101 is always configured for vector 160(8). It can be changed as described in Section 3.2.4.

4.3 User–Modifiable Parameters

As with RL Mode, the sophisticated user can change three additional parameters by modifying three locations in the low-order EPROM. The transfer block size, the step time and the maximum number of spared tracks are modified as described in Section 3.2.6. With the Extended Mode EPROMs, the default transfer block size is 32 words per burst. The maximum number of spared tracks is set at 34. In special cases, such as when fewer tracks are available, this number can be set lower, but in no case should it exceed 34.

4.4 Addressable Registers

The Extended Mode controller has the same five registers (CSR, BAR, DAR, WCR, BAE), register addresses (3ff900h - 3ff908h standard, 3ff910h -3ff918h alternate) and interrupt vector (160(8) standard and 150(8) alternate) as the RL mode controller. The register bit definitions, however, are altered slightly. The following paragraphs define the addressable register bits for Extended Mode operations.

Table 4–1. Register Addresses

LSI-11 BUS	
Hex Address	Register Name
3ff900	Control Status Register
3ff902	Bus Address Register
3ff904	Disk Address Register
3ff906	Word Count Register
3ff908	Bus Address Extension Register

4.4.1 Control Status Register

The bit functions assigned to the bits in the Control Status Register (CSR) are defined in Table 4-1.

Table 4-2. CSR Bit Description

Bit(s)	Function	Description
Bit 0	Drive Ready	This bit is used to indicate that the drive is ready. This bit is always set at command termination unless an error condition occurs or an explicit Seek command has been issued to the drive. In this case, the Get Seek STATUS will return with this bit cleared if the drive is still seeking and set if the drive is not seeking.
Bits 3-1	Command	Eight commands are encoded into these three bits. A list of the commands that can be issued in Extended Mode follows: 000 - Format and Read Bad Track Map 001 - Write Check Command 010 - Get Status Command 011 - Explicit Seek Command 100 - Read Header Command 101 - Write Command with Implied Seek 110 - Read Command with Implied Seek 111 - Get Seek Status Command (See Paragraph 4.5 for a detailed description of these commands)
Bits 5-4	not used	In the standard RL101, these bits specify bits 17 and 16 of the 18 bit LSI-11 bus address. Since Extended Mode always gets the upper six address bits from the BAE, these bits are unused.
Bit 6	Interrupt Enable	When this bit is set, the controller will interrupt at command completion.
Bit 7	Controller Ready	This bit it is cleared by the host to start command execution and set by the controller at command completion. The RL101 can be polled for completion.
Bits 9-8	Drive Select	Selects one of the four drives attached to the controller.
Bits 13-10	Error Conditions	See Table 3-4.
Bit 14	Drive Error	This bit is set when a drive hardware error is discovered during command execution.
Bit 15	Overall Error	This bit will be set any time an error condition in either bits 13-10 or a drive error in bit 14 exists.

4.4.2 Bus Address Register

The Bus Address Register's (BAR) function is unchanged in Extended Mode. Its 16 bits contain the bottom sixteen bits of the LSI-11 bus address.

4.4.3 Disk Address Register

The Disk Address Register (DAR) no longer specifies a cylinder, head and sector during read and write operations and a cylinder offset during seek operations, as it does in RL Mode. Instead, the register simply contains a logical track number during all operations (except Format and Read Bad Track Map - see the description of the Format command.) The largest logical track number that can be specified is 7ffe(h). As mentioned above, Extended Mode supports implied seek operations which means that a separate seek command does not have to be issued to get the drive to the right track before issuing the Read, Write or Write Check command. Instead, the controller will determine if the drive is at the correct place before starting a read, write or write check operation and if it is not, it will seek to the correct location before starting the read or write operation.

4.4.4 Word Count Register

In Extended Mode, the Word Count Register (WCR) is a read/write register, not write only as it is in RL Mode. The word count specified is the two's complement word count just like the RL02, except that transfers up to 64 kwords are supported in a single operation. The controller automatically advances across track and cylinder boundaries to complete a large transfer. When zero is written into the Word Count Register, a full 64K word transfer, the largest possible, occurs.

4.4.5 Bus Address Extension Register

The Bus Address Extension (BAE) register has two functions in Extended Mode. The bottom six bits of this register provide the upper six bits of the 22 bit LSI-11 bus address. Bits 10-6 of this register provide the sector number of the starting sector on which the read, write or write check operation is to take place. Bits 15-11 of this register are unused and are ignored.

4.5 Command Descriptions

Extended Mode supports these commands

Write Check
Get Status
Explicit Seek
Read Header
Write
Read
Get Seek Status
Format
Read Bad Track Map

which are described in the following paragraphs.

4.5.1 Write Check Command

The Write Check command reads data off the disk and compares it with the data in memory. Before issuing Write Check, the following information must be provided:

- The Memory Address at which the comparison is to take place is specified in the BAR and the bottom six bits of the BAE.
- The Disk Address at which the comparison is to take place is specified in the DAR (logical track number) and in bits 10-6 of the BAE (starting sector number)

- Length of the transfer in words. This is specified as a two's complement number in the WCR.

4.5.2 Get Status Command

The Get Status Command gets information about the selected drive and puts it into the following registers:

DAR - the number of logical tracks available on the drive
BAR - the number of heads available on the drive
WCR - the number of sectors per track

4.5.3 Explicit Seek Command

The Explicit Seek Command allows seeks to take place without read or write operations. The command is issued with the destination logical track number put into the DAR. Note that the Explicit Seek command returns immediately after the seek has been initiated but before it completes. The host computer can determine when the seek is complete by issuing the Get Seek Status command on the given drive.

4.5.4 Read Header Command

The Read Header Command reads the first header that comes under the currently selected head of the selected drive and places the second header word in the BAR and the third header word in the DAR. The second header word contains the Cylinder Number in bits 15-6 and the Sector Number in bits 5-0. The third header word contains the Head Number in bits 15-13 and the Logical Track Number in bits 12-0.

4.5.5 Write Command

The Write Command writes information from memory onto the disk. The user must specify the starting Memory Address, the Disk Address and the Word Count in the same manner as with the Write Check command.

4.5.6 Read Command

The Read Command reads information from disk into memory. The user must specify the starting Memory Address, the Disk Address and the Word Count in the same manner as with the Write Check command.

4.5.7 Get Seek Status Command

No parameters are required for this command. The CSR bit 0 is merely examined when the command completes. If zero, the selected drive is still seeking. If one, the selected drive is not seeking.

4.5.8 Format Command

The Format command formats a drive attached to an RL101 controller in a single operation. First, write the disk parameters for the drive to be formatted to the DAR. The contents of the DAR vary, depending upon the EPROMs. Table 4-2 and 4-3 show the DAR format when using the Extended Mode EXM2.x EPROMs and the EXM3.x EPROMs. Next, write the Format command to the CSR along with the appropriate drive selection bits, and reset the GO bit, bit 7. Refer to Section 5 for more information on the operational aspects of formatting a drive with the RL101.

Table 4-3. DAR During Format Command (EXM2.x EPROMs)

Bit(s)	Definition
Bits 9-0	The number of the maximum cylinder on the drive. When specifying this parameter, it is not necessary to allocate tracks at the end of the drive as spared tracks; the controller automatically does this. This number should be the actual largest physical cylinder number on the drive. 1023 decimal is the largest number that can be specified.
Bits 12-10	The number of the maximum heads on the drive minus one. Drives with up to eight heads are supported. For a drive with eight heads, the number would be 7.
Bit 13	Putting a one into this bit allows the user to examine the progress of formatting by examining a memory buffer beginning at location 1000(16) in physical memory. If bit 13 is set, the controller allocates a 69 word buffer at 1000(16) for status information. The layout of the buffer is defined in Table 5-1.
Bits 15-14	must be zero during formatting.

Table 4-4. DAR During Format Command (EXM3.x EPROMs)

Bit(s)	Definition
Bits 10-0	The number of the maximum cylinder on the drive. When specifying this parameter, it is not necessary to allocate tracks at the end of the drive as spared tracks; the controller automatically does this. This number should be the actual largest physical cylinder number on the drive. 2047 decimal is the largest number that can be specified.
Bits 14-11	The number of the maximum heads on the drive minus one. Drives with up to 16 heads are supported.
Bit 15	not used, must be zero during formatting.

4.5.9 Read Bad Track Map Command

The Read Bad Track command allows the user to view the hardware bad track map generated by the controller at format time and stored on the disk.

The Read Bad Track command shares command 0 in the controller CSR with the Format command. The two commands are differentiated from each other in the controller by means of bit 15 of the DAR. For the EXM2.x and EXM3.x EPROMs, write an 8000(16) to bit 15 of the DAR to execute the Read Bad Track Map command. Then write a 0 to location 774400, the CSR. Table 4-4 shows the DAR during a Read Bad Track Map command.

Table 4-5. DAR During Read Bad Track Map Command

Bit(s)	Descriiption
14-0	Don't care.
15	1 (Both EXM3.x and EXM2.x EPROMs)

The bad track map is then read from the disk and appears beginning at location 1000(16) in the host's memory. Table 4-5 shows the format of the Bad Track Map with both versions of the Extended Mode EPROMs. Frequently, no bad tracks are found on a Winchester disk during formatting. In this case, all entries in words 2-69 of the bad track map will be filled with 17777(8).

Table 4-6. Bad Track Map

Location	Function	Contents
1000(16)	Disk Parameter Word (EXM2.x EPROMs)	Bits 15-13: number of heads minus one Bits 12-0: number of logical tracks available (number of cylinders x number of heads - maximum number of tracks that can be spared.)
1000(16)	Disk Parameter Word (EXM3.x EPROMs)	Bits 15-12: number of heads minus one Bits 11-0: number of cylinders minus one
1002(16) 1004(16) ...	Bad Track Map Words (Words 2 - 69)	Each bad track occupies two word locations. The first location is the logical track which is spared. The second is the offset.
177777(8)		End of bad track map.

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SECTION 5: SUBSYSTEM OPERATIONS

5.1 Introduction

This section describes the installation of the RL101 controller and the operation of the disk subsysem, including disk formatting.

5.2 RL101 Installation

5.2.1 Checking or Replacing the EPROMs

Before installing the controller, check the EPROMs in locations 6J and 10J. Note which EPROMs are installed; programming the controller's registers depends upon the EPROM version.

When swapping EPROMs, ensure the high-order byte EPROM, designated with an H, is inserted in location 6J (EPROM socket closest to the Q-Bus connectors) and the low-order EPROM, marked L, is inserted in location 10J (EPROM socket nearest the disk drive cable connectors.)

NOTE

Make sure that both EPROMs have pin 1 oriented toward the Z8000 processor chip. Applying power to EPROMs that are incorrectly inserted may cause damage to them.

5.2.2 Dip Switches

There are two dipswitches located on the controller, as shown in Figure 3-1. Set them as appropriate.

5.2.2.1 Format Enable Switch
Switch position 1 controls Format Enable. When this switch is open, disk formatting is inhibited. An attempt to issue the RL101 Format command returns a disk drive error on the drive on which the format attempt was made. This switch prevents inadvertent formatting of a disk and lost data. When this switch is closed, disk formatting is enabled. The Read Bad Track Map command, which allows the user to examine the bad track map of a drive, executes properly with the Format Enable switch in either position.

5.2.2.2 Autoboot Enable Switch
Switch position 2 controls whether autobootstrapping of the disk occurs at power up. Autobootstrapping is a process by which the bottom block (two sectors) of disk zero are loaded into the bottom of physical memory at power up time and execution automatically starts at location 0. The LSI-11 processor must be put in the mode where it loads its initial PC and PSW from locations 24(8) and 26(8) respectively in order for autobootstrapping to occur properly. If switch position 2 is closed, autobooting occurs automatically at power up. If switch 2 is open, no autobooting occurs. See the appropriate DEC CPU technical manual for information on correctly configuring the CPU.

NOTE

When using the IS RL101 with the IS-68K board, autobooting is not enabled. Instead, the system bootstrap is contained in the PROMs on the IS-68K.

5.2.3 Cabling

The RL101 has one 34-pin and four 20-pin leaders that support from one to four ST506-compatible 5 1/4" disk drives. The 34-pin cable is daisy-chained between all 5 1/4" drives and a 20-pin cable attaches between the controller and each 5 1/4" drive. When installing the cables, be sure to observe the proper orientation of pin 1 at both ends of the cables. Normally, pin 1 on the cable is marked by a red or blue strip at one edge of the cable. In addition, a small arrowhead etched into the plastic connector normally marks pin 1. See Figure 3-1 for the location of the connectors and the orientation of pin 1 on the RL101.

5.3 Powering Up

It is recommended that the Winchester disk drives be powered up before the RL101, although this is not required. If the RL101 is powered up first, the Winchester disk drives *must* be powered up within 20 seconds. If they are not, the Winchester disks drives may not come ready within the 75 seconds allowed from power on and a Power Up Failure may result.

If possible, the flat ribbon cables should never be removed or installed from the subsystem while the subsystem is powered up. Such an event will not result in permanent disk damage but may result in non-recoverable loss of data.

5.3.1 Power–Up Failures

Four types of Power Up Failure can occur with the RL101:

1. NO DRIVES	This failure occurs when no drives are detected attached to the controller at power up time. It can also result if drives are attached to the controller, but are not powered up.
2. DRIVES NOT READY	One or more drives did not become ready in the 75 seconds alloted from power on.
3. NO HOME	could not home one or more drives in 1028 steps. (2050 steps with the EXm3.x PROMs.)
4. NO DRIVE 0	This error only occurs when autobooting is enabled and no DRIVE 0 can be found in the system. This is due to the fact that autobooting attempts to load the first two disk sectors of disk 0 into the bottom of physical memory.

If any one of these failures occur, the RL101 will never become ready and the select LED on the controller and the select light of drive 0 (provided that a drive 0 is attached to the controller) will flash a pattern (described below) to indicate to cause of failure.

5.3.2 RL101 LED Error Patterns

The RL101 Winchester controller can generate 9 different error patterns which indicate different problems that the controller has encountered. The following is a list of all the patterns possible, although some are not expected to occur in normal operation of the RL101.

0000 (short-short-short-short) NO HOME - a disk could not be homed in 1028 steps.

0001 (short-short-short-long) NOT READY - either a drive never became ready (during power up sequencing) or the drive changed from READY to NOT READY status during operation of the controller.

0010 (short-short-long-short) SEEK NOT COMPLETE - the seek did not complete on a particular drive in the maximum alloted seek time of 350 milliseconds.

0011 (short-short-long-long) NO DRIVE 0 - we could not find a DRIVE 0 at power up time. This error only occurs when autobooting is enabled and the controller attempts to load the first two sectors of DRIVE 0.

0100 POWER UP FAILURE - none of the drives attached to the controller come ready within the alloted 75 seconds after power

0101 WRITE FAULT - a write fault was detected on one of the drives.

0110 NO DRIVES - at power up, no drives could be found attached to the controller.

The following two error conditions occur during formatting only.

1010 CYLINDER 0,HEAD 0 FORMAT FAILURE - During formatting, Cylinder 0, Head 0 could not be properly formatted.

1011 TOO MANY TRACKS SPARED - During formatting, an attempt was made to spare a number of tracks greater than the maximum number permitted or specified as a supplementary parameter. By viewing the bad track map, the user can determine which tracks were spared.

5.4 Disk Formatting

The RL101 controller can format a drive and generate a bad track map without the necessity of running any software on the host computer. At the completion of formatting, the RL101 looks like one or more defect-free RL01 or RL02 disk packs, from the host point of view.

Because there is no standard for the format on Winchester disks, drives are shipped from the drive manufacturers with either no format or a format incompatible with the RL101. For this reason, the RL101 has two commands, Format and Read Bad Track Map, which replace the RLV11/RLV12 command 0, the Maintenance Mode command.

For all versions of the RL101 EPROMs, formatting is handled in the same fashion: the Disk Address Register (DAR) is written with information about the drive being formatted and the Format Command is written into the Control Status Register (CSR) along with the drive number of the drive to be formatted.

Formatting takes about one minute per megabyte. During this time, both LEDs on the controller will flash rapidly and all registers will contain 0 indicating that the controller is busy.

During formatting, data analysis is performed on all tracks of the disk by writing and reading seven different data patterns. Failure to successfully read any one of these patterns will result in that disk track being spared.

At the end of formatting, information about the disk that has just been formatted (number of heads and number of cylinders) is stored on that disk along with the bad track map that has been generated by the controller while formatting. The Read Bad Map Command can be used to view this bad track map.

5.4.1 Writing the DAR

First, ensure Switch 1, the Format Enable dipswitch, is in the closed position. Next, write the disk format parameters for the drive to be formatted to the DAR. The contents of the DAR for formatting vary, depending upon the type of disk being formatted and the version of the EPROMs used by the controller, as described in Section 3 for RL Mode controllers, and Section 4 for Extended Mode controllers. The disk specific parameters, such as the number of heads and cylinders, vary among drives. Appendix A shows these parameter values for selected disk drives.

5.4.2 Writing The CSR

Finally, before formatting begins, enter command 0 in the CSR along with the appropriate drive selection bits and reset bit 7, the GO bit. For example, to initiate formatting on drive 0, the contents of the CSR would be written to 0(8); to initiate formatting on drive 1, the contents would be written to 400(8). With the 4L EPROMs, which support one physical drive only, it is always appropriate to select drive 0.

5.4.3 Status Information During Formatting

With the EXM and 4L versions of the EPROMs, it is possible to monitor formatting progress. (Regardless of the EPROM version, the controller automatically writes status information and the bad track map to the disk, at the completion of formatting. The Read Bad Track Map Command is described in Section 3.5.9 (RL Mode) and Section 4.5.9 (Extended Mode.) With the Extended Mode EXM3.x EPROMs, the controller automatically allocates a 69-word formatting status buffer starting at host memory location 1000h. With the RL Mode 4L EPROMs and the Extended Mode EXM2.x EPROMs, this buffer is allocated if bit 13 of the DAR is a "1".

The format of this status buffer is shown in Table 5-1. At locations 10002(8), 10006(8), 10010(8), etc. the logical track numbers of any tracks that can be spared can be observed as they are spared. At locations 10004(8), 10008(8), etc. the offsets associated with the preceeding logical track can be observed. Note that the end of the bad track map is indicated by a location of all 1s (ie 177777(8)). The entire bad track status area in memory is filled with this value before formatting is started. For example, a typical bad track status area might look as follows during formatting:

```
10000/ 12
10002/ 573
10004/ 1
10006/ 1221
10010/ 2
10012/ 177777
10014/ 177777
```

The first location of the bad track status indicates that cylinder 122(8) is being formatted currently. The second and third locations mean that all logical tracks between 573 and 1221(8) have one added to them to get the physical track number. All logical tracks greater than or equal to 1221 have 2 added to them. The 177777(8) in location 10012 means the end of the bad track map and that only two bad tracks have been found at this point in the formatting. As more bad tracks are found during formatting, they will be added to the bad track map.

Table 5-1. Status Buffer During Formatting (4L and EXM EPROMs)

Location	Contents
10000(8)	the number of the cylinder that is currently being formatted.
10002(8)	the current bad tracks in the following format: Odd words beginning with location 10002: (i.e. 10002, 10006, 10000a) the starting logical track above which the corresponding offset (following location) must be applied to get to the physical track. Even words beginning with location 10004: the track offset, the number that must be added to the logical track number to get to the correct physical track number

5.4.4 Successful Completion of Formatting

Upon successful completion of the disk formatting operation, the formatted drive is homed, and the bad track map is written redundantly on the first three sectors of cylinder 0, head 0, which is accessible to the user through the Read Bad Track Map Command. In addition, the bad track information, left in host memory location 10000(8) and described previously, is still available for examination.

Once formatting completes successfully, reset Switch #1, the Format Enable dipswitch, to the open position. When the switch is open, disk formatting is inhibited. This switch setting prevents inadvertent formatting and lost of data.

Also, the controller must be reset before the newly-formatted drive will operate properly. When the controller is reset, the newly-written bad track map is reloaded into the proper location of the controller's RAM. The easiest way to reset the controller is to press BOOT or RESET on the computer's console. If the computer does not have either of these switches, the power must be cycled.

5.4.5 Reading The Bad Track Map

The Read Bad Track command allows the user to view at any time the hardware bad track map generated by the controller at format time and stored on the disk. A description of this command and the Bad Track Map generated by it can be found in Section 3 (RL Mode controllers) or Section 4 (Extended Mode controllers)

5.4.6 Unsuccessful Completion

The formatting operation can terminate unsuccessfully for one of three reasons:

- Format Enable Switch Disabled - The format enable switch must be closed for formatting to begin. The controller will return immediately with a drive error on the drive being formatted if the Format Enable Switch is not closed.
- Inability to Properly Format Cylinder 0, Head 0 - Information critical to the proper operation of the RL101 is stored on cylinder 0, head 0 of each disk. It is a requirement

for proper formatting that cylinder 0, head 0 be able to be formatted properly. If not, the controller will terminate formatting and flash the long-short-long-short pattern on the controller select light and on Drive 0. This pattern will continue indefinitely until the controller is powered down. Because cylinder 0, head 0 is the first track that is formatted, this failure will occur within five seconds of the start of formatting if it is going to occur at all.

- Too Many Tracks Spared - The number of tracks that can be spared on each disk is a function of two parameters, the absolute limit supported by the firmware and a possible smaller number stored as a supplementary parameter into the controller firmware. With the RL101, 2L, 4L, EXM.x EPROMs shipped from the factory, the supplementary parameter is always the same as the firmware's absolute limit. For the RL101 and 2L EPROMs, this limit is 12 tracks; for the 4L EPROMs and the Extended Mode EXM EPROMs, this limit is 34 tracks. Whenever the number of tracks spared by the RL101 exceeds the number permitted, the controller will write the bad track map to disk and then stop operation, flashing the long-short-long-long pattern to indicate that too many tracks have been spared.

5.4.6.1 Troubleshooting Hints

The proper action to take upon a format failure depends on the failure indication. The failure of the controller to initiate formatting and the disk error return usually indicates that the Format Enable switch is not enabled. Another possible cause is that the disk on which a format is being attempted is not properly connected to the controller. Be sure to observe the pin 1 indications on the controller to Winchester disk cabling.

Inability to properly format Cylinder 0, Head 0. This is almost always caused by a cabling error or a write protect switch being set on the drive on which a format is being attempted. In some very rare cases, this error could result from a legitimate hard failure on cylinder 0, head 0. In this case, the user has no choice but to exchange the particular disk drive for another unit.

NOTE

Almost all 5 1/4" Winchester drive manufacturers specify that either Cylinder 0, Head 0 or in most cases all of cylinder 0 will be error free. If a hard error is occuring on cylinder 0, head 0, check your Winchester disk drive users manual. There is a high probability that this drive is violating the manufacturers specifications.

Too Many Tracks Spared - The most common reason for this error to occur is that one of the two disk parameters specified to the controller in the DAR has been incorrectly specified. If the number of heads has been specified to be greater than the number of heads that actually exist on the disk, then the tracks corresponding to non-existent heads will be spared until the maximum number permitted is exceeded. Another common reason for this error is that the drive does not have as many cylinders as specified in the Format command. Again, to emulate the RL01, 641 tracks plus the number of spares allowed are required while to emulate the RL02, 1281 tracks plus the number of spares required are required. For the standard sparing limit of 12 tracks, the requirement would be 652 tracks for the RL01 emulation and 1292 tracks for the RL02 emulation.

APPENDIX A: DISK PARAMETERS FOR SELECTED DRIVES

A.1 About This Appendix

This appendix contains formatting constants for a selected group of disk drives supported by the RL101 controller. The tables are not complete nor are they an endorsement of any drive or drive manufacturer.

TABLE OF DRIVES AND FORMATTING CONSTANTS
RL Mode (4L EPROMs)

Mfg.	Drive Type	# of Heads	# of Cylinders	Minimum Step Time	Formatting Constant DAR	Looks Like
CDC	WREN 9415-3	3	697	8	2AB8	1 RL02
	WREN 9415-5	5	697	8	32B8	2 RL02
Maxtor	1065	7	918	1	3B95	4 RL02
	1105[1]	11	918	1	x	-
	1140[1]	15	918	1	x	-
Quantum	520	4	512	3	2DFF	1 RL02
	530	6	512	3	35FF	2 RL02
	540	8	512	3	3DFF	3 RL02
Rhodine	204	8	322	10	3D41	2 RL02
Ampex	Pyxis 27	8	322	10	3D41	2 RL02
Fujitsu	M2241	4	754	3	2EF1	2 RL02
	M2242	7	754	3	3AF1	4 RL02
	M2243[1]	11	754	3	x	-

1 Not supported by 4L EPROMs - more than eight heads.

TABLE OF DRIVES AND FORMATTING CONSTANTS
Extended Mode

Mfg.	Drive Type	# of Heads	# of Cylinders	Minimum Step Time[1]	Formatting Constant EXM2.x DAR	EXM3.x DAR
CDC	WREN 9415-3	3	697	8	2AB8	12B8
CDC	WREN 9415-5	5	697	8	32B8	22B8
Maxtor	1065	7	918	1	3B95	3395
	1105	11	918	1	x	5395
	1140	15	918	1	x	7395
Quantum	520	4	512	3	2DFF	19FF
	530	6	512	3	35FF	29FF
	540	8	512	3	3DFF	39FF
IMI	5006H[2]	2	322	3	2541	0941
	5012H	4	322	3	2D41	1941
	5018	6	322	3	3541	2941
Rhodime	202	4	322	10	2D41	1941
	203	6	322	10	3541	2941
	204	8	322	10	3D41	3941
Ampex	Pyxis 13	4	322	10	2D41	1941
	Pyxis 20	6	322	10	3541	2941
	Pyxis 27	8	322	10	3D41	3941
Seagate	ST412	4	306	25	2D31	1931
	ST419	6	306	25	3531	2931
Fujitsu	M2241	4	754	3	2EF1	1AF1
	M2242	7	754	3	3AF1	32F1
	M2243	11	754	3	x	52F1

x - Not supported by REV 2.x proms - more than eight heads.

1 - As long as the minimum step time is less than or equal to 10 microseconds, the default RL101 rate of 10 microseconds per step will work satisfactorily.

2 - The IMI drives specify some number of cylinders beyond 306 being available as spares. Consultation with IMI determined that 322 cylinders would always be available.

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